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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
HUR, JUNG H	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JANG-WON MOON, SUNG-HOON KIM, KYOUNG-HO KIM, JOUNG-YEAL KIM, and HO-YOUNG SONG

Appeal 2009-0219
Application 10/715,015
Technology Center 2800

Decided[1]: March 4, 2009

Before JOSEPH F. RUGGIERO, MAHSHID D. SAADAT, and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R.§ 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1, 4-10 and 15-16. Claims 2-3 have been cancelled and claims 11-14 have been objected to as being dependent upon a rejected base claim, but otherwise allowable. (App. Br. 1-2).[2] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants invented, according to their disclosure, a precharge circuit that generates first and second delay signals from a column bank address (CBA) signal. The precharge circuit allows data lines in a memory circuit to be charged after either a read or write operation. The two delay signals are selectable based on the state of a write enable signal (PWR), thereby allowing for different precharge times as required after the read and write operations. (Spec. Abstract, Fig. 2).

Exemplary claim 1 follows:

1. A memory device, comprising:

a data line; and

a variable delay precharge circuit that receives a column bank address signal and a write enable signal and that precharges the data line responsive to the column bank address signal at a time that is determined by a state of

[2]Appellants' Brief (filed June 19, 2006) ("App. Br.") and Supplemental Brief (filed September 13, 2007 ("Supp. App. Br."), and the Examiner's Answer (mailed October 12, 2007) ("Ans."), detail the respective positions of the parties.

the write enable signal, wherein the variable delay precharge circuit comprises:

a precharge circuit operative to precharge the data line responsive to a precharge control signal;

a precharge control signal generator circuit that receives the column bank address signal, that generates first and second delayed signals from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal, and that applies to the precharge circuit, responsive to a precharge delay control signal, a selected one of a first precharge control signal generated from the first delayed signal and a second precharge control signal generated from the second delayed signal; and

a precharge delay control circuit that generates the precharge delay control signal responsive to the write enable signal.

The Examiner relies on the following prior art references:

Yu	US 5,828,612	Oct. 27, 1998
Nitta	US 5,831,924	Nov. 3, 1998

Admitted Prior Art ("APA"), Figures 1A and 1B and Spec. 1: 22 – 2:23.

The Examiner rejected claims 1, 4-7, 9, 10, 15 and 16 under 35 U.S.C. § 103(a) based upon Appellants' admitted prior art ("APA") and Yu.

The Examiner rejected claim 8 under 35 U.S.C. § 103(a) based upon the APA, Yu, and Nitta.

ISSUE

The arguments provided by Appellants and the Examiner present the following issue: Did Appellants demonstrate that the Examiner erred in finding that that the APA and Yu collectively teach "a precharge control signal generator circuit that receives the column bank address signal, that generates first and second delayed signals from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal," as set forth in representative claim 1?[3]

FINDINGS OF FACT (FF)

1. Appellants admit, in the "Background Art" section of their Specification, (i.e., APA), that column bank address signals (CBA) are used to generate a delayed precharge control signal after data is read and after data is written. (Spec. 1: 22 – 2:23; Figs. 1A, 1B).

2. Yu's control circuit 14 generates different precharge signals as a function of an address signal Ax for a memory array, a clock CLK, a sense enable signal SAEN, and an R/W (read/write) enable signal. The control circuitry controls the amount of time sense amplifiers perform a sense operation, ultimately determining when the sense enable signal occurs to signify the end of a read operation so that precharging occurs. The control circuitry performs precharging only between read and write operations. The precharge signal is asserted and de-asserted at different times depending on

[3] Appellants group independent claims 1, 6, 9 and 15 together, and do not present separate patentability arguments for the remaining claims. Therefore, claim 1 is representative. *See* 37 C.F.R. § 41.37(c)(1)(vii).

whether a read or write operation is performed. Read and write operations require an address signal so that the correct memory row and column of a memory array 26 can be addressed. The precharge signal 110 also requires a correct bit line address to precharge the correct bit lines. (Yu, col. 3, ll. 31-67; col. 4, l. 35 to col. 5, l. 21, Abstract; Figs 1-4).

3. Yu discloses at least two distinct delayed precharge control signals, t2, and t5, generated at the same time as the trailing edge of a clock signal (CLK 104) and a change in an address signal Ax. (Fig. 3).

4. Yu teaches that such distinct delays associated with different precharge signals after read and write operations provide faster memory operations due to increased recovery time, because write operations require longer precharge times. (Col. 1, l. 46 to col. 2, l. 21).

5. Yu's distinct delay signals t2 and t5 are generated in response to a R/W 102 enable condition which signifies either a read or write operation. Selection of the distinct delays also depends on the state of other signals, including *inter alia*, the clock 104, the write precharge trigger 212, and the default precharge trigger 216. (Yu, Figs. 3, 4).

6. The periods t2 and t5 correspond to different precharge operation begin and/or end times at precharge output 110, including the last two right-hand "PRECHARGE" times at 110, as signified by arrows to and from the time periods t2 and t5 to the different PRECHARGE time periods. (Fig. 3) The periods t2 and t5 define delayed periods relative to the trailing edge of the clock 104, which coincides with address changes, signified as Ax 101, after read and write operations, which are determined in part by the write enable signal R/W 102. (Yu, col. col. 8, l. 58 to col. 9, l. 42, Fig. 3).

PRINCIPLES OF LAW

"[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). "On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness." *In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)). To establish a prima facie case,

> "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

> [W]hen a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result....
>
> ....
>
> ...For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* and *Anderson's-Black Rock* are illustrative – a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740 (citations omitted).

"[O]ne cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references". *In re Keller*, 642 F.2d 413, 426 (CCPA 1981).

ANALYSIS

Appellants argue that the APA does not disclose different first and second delay signals and that Yu only discloses a default precharge signal responsive to an address signal, and therefore, fails to suggest claim 1. (App. Br. 5). However, the Examiner (Ans. 3-5) rejected claim 1 based on the combined teachings of the APA and Yu. Under *Keller*, Appellants' separate arguments against the reference teachings do not defeat obviousness.

The Examiner reasoned (Ans. 3-5) that Yu teaches two signals t2 and t5 delayed by different amounts and generated pursuant to a clock signal, while the APA teaches two signals delayed by the same amount and generated pursuant to a CBA (column bank address) signal. These findings are supported (FF 1-6) and unchallenged by Appellants. Based on these findings, the Examiner reasoned (Ans. 3-5) that it would have been obvious to employ the APA CBA signal in place of Yu's clock signal to increase the frequency of operation, thereby meeting the claim limitation. Under *KSR* and *Kahn*, substitution of one prior art trigger signal for another, where each performs its expected purpose of generating delay signals and the combination predictably benefits the system by decreasing the operating time (*see* FF 4), constitutes a prima facie case of obviousness.

Further, any memory address read and write circuit requires a clock. Appellants' disclosure does not provide the implied relationship between the

clock and the memory column bank address (CBA) recited in the claim. However, implicit in the claimed invention, and explicit in Yu, is the fact that a memory array (*see e.g.,* Yu's memory array 26 at Fig. 1), necessarily having rows and columns, requires a correct address signal relative to a clock signal. Row and column (CBA) address signals are also required for read, write and precharge operations. (FF 2). Moreover, Yu's address signal Ax and clock (CLK 104) in Figure 3 are synchronized together when the address changes at the clock edges. The two distinct delay signals, t2 and t5, meeting the claim according to the Examiner (Ans. 4, 5, 7, 8), start relative to that synchronized clock edge and therefore define delays relative thereto (*see* FF 2, 5, 6). As the Examiner found, Yu's two distinct delay signals t2 and t5 are delayed relative to the clock signals (Ans. 4, 5, 7, 8). However, since the clock signals 104 and address signals Ax are synchronized, it follows that the two delay signals also are delayed relative to an address signal Ax. (FF 3, 5, 6, *see* Yu, Fig. 3).

Further, first and second precharge control signals (*see* the at least two distinct "PRECHARGE" conditions depicted at output line 110 in Yu at Figure 3) are applied to the precharge circuit, i.e., at the output of 110 (*see also*Yu, Fig. 2). The first and second control signals are generated from, *inter alia*, the delay signals associated with t2 and t5. The precharge generator circuit 14 (Yu, Fig. 1) receives a column bank address signal Ax, and generates, at least, the first and second delay signals t2 and t5 with respect to Ax. A precharge delay control signal at the output of NAND gate 306 is ultimately responsive to the write enable signal 102 (Yu, Fig. 2). (*See* FF 2-6). Thus, Yu, at a minimum, suggests employing the column bank address signal as recited in claim 1, as generally found by the Examiner.

Appellants fail to meet the burden of demonstrating error in the Examiner's prima facie case of obviousness. Merely repeating claim limitations and stating that the references fail to teach the limitations, or that motivation lacks, as Appellants do (App. Br. 5-7), does not rebut the Examiner's prima facie case.

In view of the above discussion, we will sustain the Examiner's 35 U.S.C. § 103 rejection of claim 1, and claims 4-7, 9, 10, 15 and 16 which are grouped with claim 1. We also will sustain the Examiner's rejection of claim 8, based on the additional Nitta reference, because Appellants rely on the same arguments asserted for claim 1.

CONCLUSION

Appellants did not demonstrate that the Examiner erred in finding that that the APA and Yu collectively teach "a precharge control signal generator circuit that receives the column bank address signal, that generates first and second delayed signals from the column bank address signal that are delayed by respective different first and second time periods with respect to the column bank address signal," as set forth in representative claim 1.

DECISION

We affirm the Examiner's decision rejecting claims 1, 4-10, 15, and 16.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv)(2006).

AFFIRMED

gvw

MYERS BIGEL SIBLEY & SAJOVEC
P. O. BOX 37428
RALEIGH, NC 27627